FAX

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FACSIMILE TRANSMITTAL LEGEND------>

MESSAGE

Re: Ser. No. 09/870,531
filed 31 May 2001
Attorney Docket No.: FIS9-2000-0412-US1

Following the cover sheet are the original Transmittal Form plus the last five pages of a facsimile transmission in the above application which were being sent. Apparently the transmission was interrupted through no fault of my own during transmission about 8:50 PM last night. It is believed that the only pages missing were the marked copies of the amendments. The failure in transmission was discovered this morning about 10AM.

Respectfully submitted,

Graham S. Jones, II
Reg. No. 20,429

Date: 5/06/03 Pages: 1 of

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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/870,531
Filing Date	31 May 2001
First Named Inventor	Peter J. Brofman
Group Art Unit	2815
Examiner Name	James M. Mitchell
Total Number of Pages In This Submission: 17	Attorney Docket Number: FIS9-2000-0412-US1

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Graham S. Jones, II, Reg. No. 20,429
Signature	
Date	5 May 2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being sent by Facsimile to the Commissioner for Patents on this date to the Facsimile transmission Number 703-872-9318 . 5 May 2003

Typed or printed name	Graham S. Jones, II		
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Serial No.:	09/870,531	Art Unit:	2827

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend the paragraph [0007] beginning at page 3, line 1 to read as follows:

- -[0007] U.S. patent No. 6,184,060 of Siniaguine for "Integrated Circuits and Methods for Their Fabrication" describes **formation of vias and** contact **pads** **[~~vias formed~~]** on the back side of a silicon semiconductor chip. The vias **and contact pads** are formed by the process starting with forming tapered vias (openings) in the back of a workpiece comprising a silicon wafer by with an isotropic plasma etch of the via opening down into the silicon wafer through an aluminum or photoresist mask formed over the silicon. The via openings **have** **[~~has~~]** a depth at least as large as the final thickness of the wafer after the manufacturing process is completed. After the mask is removed, a thin conformal, glass or BPSG dielectric layer (1-2 μm thick) is formed over the substrate including the vias. Then a thin conformal blanket conductive layer (e.g. 0.8-1.2 μm thick) is formed over the dielectric layer of aluminum, gold or nickel. A planar glass layer is spun onto the surface of the conductive layer to fill the vias to provide a planar top surface of the wafer. The conductive layer may or may not have been patterned before the last step of filling the vias with the planar glass layer. Other layers to be a part of the device structure are then formed on top of the planarized surface of the workpiece including a dielectric layer and contact pads. Then the back side of the silicon wafer is etched by an atmospheric plasma etch with argon and carbon tetrafluoride in air. When the glass or BPSG dielectric layer becomes exposed, **the** silicon substrate is preferentially etched relative to the silicon dioxide **dielectric** layer by almost an order of magnitude difference with the silicon etching far more quickly. **[The] Thus, the portions of the** lower surface (back side) of the **conductive layer formed in the** via **openings** comprise contact pads for the back side of the chip **which are exposed by the preferential etching away of the silicon**. - -